

Department of Electronics & Communication Engineering

M.M.M. Engineering College, Gorakhpur

RESEARCH PUBLICATIONS (01 January 2007 to till Date)

Date: 04/10/2010

International Conference:

1. "Design of a High Speed SiGe HBT for Wireless Applications," R.K. Chauhan, presented at International Conference IICT-2007 held at DIT, Dehradun on 27-28, July 2007.
2. "Performance Analysis of a Bandgap Engineered Silicon Bipolar Transistor," R.K. Chauhan, Proceedings of *Emerging Trends in Electronic and Photonic Devices and Systems*, pp. 79-82 an International Conference organized by IT, BHU (**Electro-2009**) from 22-24, December, 2009.
3. "Electrical Parameter Characterization Of Bandgap Engineered Silicon Germanium Hbt For Hf Applications," R.K. Chauhan, International Conference on Signal Processing and VLSI held at Hyderabad from 11-13th June, 2010.
4. "Performance Analysis of SiGe:C HBT" R.K. Chauhan, Proceedings of ICCCT-2010, pp. 314-317, held at MNNIT-Allahabad from 17th to 19th Sept, 2010.
5. "A Fault-tolerant Switching System For Next-generation Computer Networks", V.S. Tripathi, *Proc. International Conference on Information and Communication Technology (IICT, 2007)*, , pp. 173-178, July 26 –28, 2007.

National Conference:

1. Programmable Input and Output Resistances; B.P.Singh. National Conference on IT Research and Applications, pp.68-70, MAIMT, Jagadhri, Yamunanagar, Haryana. Nov.16th to 18th, 2007.
2. FFT Butterfly Realization Using Hybrid Signed Digit Number System, B.S. Rai, Proceeding of 2nd ISSS National Conference on MEMS, Microsensor, Smart Materials, Structures and Systems, CEERI BITs Pilani (India) Nov. 16.17, 2007.

3. FFT-Butterfly Realization using signed digit number system; B.S. Rai, Proceeding ICETAET 2008, Rajkot, Gujrat, pp.1750-1763,13-14 Jan 2008.
4. FFT Realization using Hybrid Signed Digit Number System; B.S. Rai, IInd ISSS National Conference on MEMS, MICROSENSORS, SMART MATERIALS, STRUCTURE & SYSTEM Proceeding ICETAET 2008, Rajkot Gujrat pp.1750-1763, 13-14 Jan 2008.
5. VHDL Realization of 32-point DIT-FET Processor Using SD2 number system, B.S. Rai, proceeding on National Seminar on information, communication and Intelligent system. IETE Cochin pp 24-31,8-9 Feb.2008.
6. "Single Walled Carbon Nanotubes (SWCN) and its Application: A Review," R.K. Chauhan, *Workshop on Nanotechnology in Semiconductor Industry*,. pp. 16-25, held at MMMEC-Gorakhpur. 5-6, April, 2008
7. "Nanotechnology in Electronics: Goals and Challenges," R.K. Chauhan, *Workshop on Nanotechnology in Semiconductor Industry*. pp. 5-13, held at MMMEC-Gorakhpur , 5-6, April, 2008
8. "Performance Analysis of an Asymmetric Metal-Semiconductor-Metal Photodetector," R.K. Chauhan, IEEE sponsored National Workshop on Advanced optoelectronic materials & devices (**AOMD-2008**), held at Center for Research in Microelectronics, Department of ECE, I.T., B.H.U., Varanasi, pp. 197-200, 22nd -24th December, 2008.
9. "Performance evaluation of strained Si/SiGe n-channel MOSFET" R.K.Chauhan, Proceedings of the National conference on Emerging Technologies (**NCET-2009**), organized by MIT, Moradabad, , pp. 381-385, 24th -25th January-2009.
10. "Design of a High Gain Darlington Amplifier for Microwave Applications," R.K. Chauhan, National Conference on Cutting Edge Computer and Electronics Technologies, **[(CE)²T-2009]** held at College of Technology, G.B.Pant University of Ag & Technology, Pantnagar from, pp. 435-437, 14-16 Feb, 2009.
11. "Challenging Issues in the Design and Development of SiGe MEMS Technology" R.K. Chauhan, Proceedings of National Conference (**RTME-2009**) organized by MMMEC-2009 on 12-13 October, 2009.

Journals:

1. Development of Fast Binary Square Rooting Algorithm, B.S. Rai Journal of Current Sciences.12 (2):pp.421-428, 2008.
2. "Development of New Interactive Methods for Performing Binary Square Resting Rapidly by utilizing Multiplications" B.S. Rai, Journal of current science 12(2) pp.499-503, 2008.
3. "A New Profile Design for Silicon Germanium based Hetero-Junction Bipolar Transistors," R.K. Chauhan, *Journal of Computational and Theoretical Nanosciences*, Vol.5 (11), pp. 2238-2242,.(American Scientific Publishers, U.S.A) Nov 2008.
4. "Effect of Ge Profile Design on the Performance of an n-p-n SiGe HBT Based Analog Circuits," R.K. Chauhan, *Microelectronics Journal*, **39(12)**, pp. 1770-1773, Dec 2008. (Elsevier Publications,U.K)

(C. B. Tripathi)

Professor & Head